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INFORMATION DISCLOSURE STATEMENT BY APPLICANT			Substitute for form 1449A/PTO		
			Complete if Known		
			Application No.	10/749,912	
			Filing Date	December 30, 2003	
			First Named Inventor	Donald E. Steiss	
			Art Unit	Not Yet Known	
Examiner Name	Not Yet Known				
Attorney Docket Number	22347-08261 (Seq. No. 8117)				
Sheet	1	of	3		

U.S. PATENT DOCUMENTS				
Examiner Initials*	Cite No. ¹	Document No. Number - Kind Code ² (if known)	Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
J		US-5,613,114	03-18-1997	Anderson et al.
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		US-6,016,542	01-18-2000	Gottlieb et al.
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	US-6,490,612	12-03-2002	Jones et al.	

Examiner Signature	<i>Jacob P. ...</i>	Date Considered	3-22-06
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U.S. PATENT DOCUMENTS				
Examiner Initials*	Cite No. ¹	Document No. Number - Kind Code ² (if known)	Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
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Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶

OTHER REFERENCES – NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ⁶
P	C1	Boothe, B. and Ranade, A. G., "Improved Multithreading Techniques for Hiding Communication Latency in Multiprocessors," ACM 1992, pp. 214-223.	

Examiner Signature	<i>Jacob Behrman</i>	Date Considered	3-22-06
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OTHER REFERENCES – NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
J	C2	Gulati, M. and Bagherzadeh, N., "Performance Study of a Multithreaded Superscalar Microprocessor," 2 nd International Symposium on High-Performance Computer Architecture, February 1996, 11 pages.	
	C3	Loikkanen, M. and Bagherzadeh, N., "A Fine-Grain Multithreading Superscalar Architecture," Proc. 1996 Confer. Parallel Architectures and Compilation Techniques, October 1996, 6 pages.	
	C4	Tullsen, D. M. et al., "Exploiting Choice: Instruction Fetch and Issue on an Implementable Simultaneous Multithreading Processor," Proc. Of the 23 rd ISCA, May 1996, 12 pages.	
	C5	Tullsen, D. M. et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proc. Of the 22 nd ISCA, June 1995, 12 pages.	
	C6	Yamamoto, W., "An Analysis of Multistreamed, Superscalar Processor Architectures," Ph.D. Thesis, U.C. Santa Barbara, Dec. 1995, pp. 1-155.	

Examiner Signature	<i>Jacob Petrucci</i>	Date Considered	3-22-06
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